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EXAMINER	
KALAM, ABUL	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,018	TOKANO ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5-8,10,11 and 17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, Embodiment I (claims 1-4, 9, and 12-16) in the reply filed on May 12, 2006 is acknowledged.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claims 1-4, 9, and 12-16 are objected to because of antecedent basis issues.

In lines 19-20 of claim 1, the limitation "the first conductivity type semiconductor layer" is unclear because of antecedent basis problems. Is the limitation, "the first conductivity type semiconductor layer," referring to one of the two, previously claimed, "first conductivity type semiconductor layers," or is the limitation referring to both of "the first conductivity type semiconductor layers." The same issue also exists in line 33 of claim 1, lines 3-4 of claim 2, lines 2-3 of claim 3, and line 9 of claim 15. Claims 2-4, 9, and 12-16 depend from claim 1, and thus are also objected to.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In lines 2-4 of claim 14, the limitation "the semiconductor structure that is partially separated from the unit cell by the separating member," is indefinite because the limitation is conflicting with the limitation "the unit cell comprising: a semiconductor structure," which is in lines 9-10 of claim 1. Is the semiconductor structure of claim 14 different from the semiconductor structure of claim 1?

In line 22 of claim 15, the limitation "is set to 10 μm or more," is unclear because it is difficult to determine the feature of the claim this limitation is referring to. Is this limitation restating the earlier limitation in which "the source electrode on the termination region side extends 10 μm or more," or is this limitation referring to "the first conductivity type semiconductor layer?" Claim 16 depends from claim 15, and thus contains the same error.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Izumisawa et al. (US 6,878,989).

With respect to claim 1, Izumisawa teaches a semiconductor device (figs. 1 and 14A) comprising:

a first conductivity type (N-type) semiconductor substrate (11);

a vertical unit cell that employs the first conductivity type semiconductor substrate as a first conductivity type drain layer (fig. 1); and

a separating member (21, 22) formed on the first conductivity type semiconductor substrate, separating the unit cell from other element,

the unit cell comprising:

a semiconductor structure comprising three semiconductor layers (19, 20) selectively formed on a main surface of the first conductivity type semiconductor substrate,

the three semiconductor layers including a second conductivity type (P-type) semiconductor layer (20) and two first conductivity type semiconductor layers (19)

formed to interpose the second conductivity type semiconductor layer from both side surfaces (fig. 1),

a p-n junction boundary between the second conductivity type semiconductor layer and the first conductivity type semiconductor layer (20 and 19) (as best interpreted by the Office) being substantially vertical to the main surface of the first conductivity type semiconductor substrate (pg. 3, [0054]),

a second conductivity type base layer (26) formed on an upper surface of the second conductivity type semiconductor layer (20) and having an impurity concentration higher than the second conductivity type semiconductor layer (pg. 5 [0080]);

a first conductivity type source diffusion layer (27) selectively formed on a surface of the second conductivity type base layer (26);

a gate insulating film (29) formed on the second conductivity type base layer (26) interposed between the first conductivity type source diffusion layer (27) and the first conductivity type semiconductor layer (19) (as best interpreted by the Office), and

a gate electrode (28) formed on the gate insulating film (pg. 2, [0052]-[0056]).

With respect to claim 3, Izumisawa teaches the semiconductor device of claim 1, as set forth above, wherein the first conductivity type impurity in the first conductivity type semiconductor layer (19) (as best interpreted by the Office) is arsenic and the second conductivity type impurity in the second conductivity type semiconductor layer (20) is boron (pg. 4, [0062]).

With respect to claim 4, Izumisawa teaches the semiconductor device of claim 1, as set forth above, wherein an inequality: (100* |A-B|/A is greater than or equal to 5) is

satisfied where A represents a total amount of a second conductivity type impurity in the second conductivity type semiconductor layer and B represents a total amount of a first conductivity type impurity in the two first conductivity type semiconductor layers (pg. 4, [0062]).

3. Claims 1, 2, 4 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Onishi et al. (US 2001/0028083).

With respect to claim 1, Onishi teaches a semiconductor device (figs. 1b) comprising:

a first conductivity type (N-type) semiconductor substrate (11);

a vertical unit cell that employs the first conductivity type semiconductor substrate as a first conductivity type drain layer (fig. 1b); and

a separating member (boundary between 20aa and 22bb) formed on the first conductivity type semiconductor substrate, separating the unit cell from other element (pg. 4, [0057]),

the unit cell comprising:

a semiconductor structure comprising three semiconductor layers (22a, 22b) selectively formed on a main surface of the first conductivity type semiconductor substrate,

the three semiconductor layers including a second conductivity type (P-type) semiconductor layer (22b) and two first conductivity type semiconductor layers (22a)

formed to interpose the second conductivity type semiconductor layer from both side surfaces (fig. 1b),

a p-n junction boundary between the second conductivity type semiconductor layer and the first conductivity type semiconductor layer (20 and 19) (as best interpreted by the Office) being substantially vertical to the main surface of the first conductivity type semiconductor substrate (pg. 4, [0055]),

a second conductivity type base layer (13a) formed on an upper surface of the second conductivity type semiconductor layer (22b) and having an impurity concentration higher than the second conductivity type semiconductor layer (pg. 5 [0054]);

a first conductivity type source diffusion layer (14) selectively formed on a surface of the second conductivity type base layer (13a);

a gate insulating film (15) formed on the second conductivity type base layer (13a) interposed between the first conductivity type source diffusion layer (24) and the first conductivity type semiconductor layer (22a) (as best interpreted by the Office), and

a gate electrode (16) formed on the gate insulating film (pg. 4, [0054]-[0059]).

With respect to claim 2, Onishi teaches the semiconductor device according to claim 1, as set forth above, wherein a concentration of a first conductivity type impurity in the first conductivity type semiconductor layer (22a) (as best interpreted by the Office) is 3 to $18*10^{15}$(atoms/cm^3) and a concentration of a second conductivity type impurity in the second conductivity type semiconductor layer (22b) is 0.2 to $8*10^{15}$(atoms/cm^3) (pg. 7, [0094]).

With respect to claim 4, Onishi teaches the semiconductor device according to claim 1, as set forth above, wherein an inequality: (100 * |A-B|/A is greater than or equal to 5) is satisfied where A represents a total amount of a second conductivity type impurity in the second conductivity type semiconductor layer and B represents a total amount of a first conductivity type impurity in the two first conductivity type semiconductor layers (pg. 7, [0094]).

With respect to claim 15, Onishi teaches the semiconductor device according to claim 1, as set forth above, wherein a plurality of unit cells identical to the unit cell are formed such as to employ the first conductivity type semiconductor substrate (11) as a common first conductivity type drain layer (fig. 1b),

a termination region (20) for the element region that contains the unit cells is separated from the element region by the separating member (boundary between 20aa and 22bb),

the first conductivity type semiconductor layer (22a) (as best interpreted by the Office) and the second conductivity type semiconductor layer (22b) are further formed in line on a side surface of the separating member on the termination region side (20ab, 20b);

a source electrode (17) is formed such as to be in contact with each of the first conductivity type source diffusion layers (14) of the unit cells; and

an end portion of the source electrode on the termination region side extends 10μm or more than an end portion on the termination region side of the first conductivity type semiconductor layer (20aa, fig. 27) further formed on the side surface of the

separating member on the termination region side is set to 10μm or more (pg. 16, [0190]) (as best interpreted by the Office).

4. Claims 1, 2, 4, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al. (US 2003/0222327).

With respect to claim 1, Yamaguchi teaches a semiconductor device (fig. 12) comprising:

a first conductivity type (N-type) semiconductor substrate (20);

a vertical unit cell that employs the first conductivity type semiconductor substrate as a first conductivity type drain layer (fig. 12); and

a separating member (64, 66) formed on the first conductivity type semiconductor substrate, separating the unit cell from other element,

the unit cell comprising:

a semiconductor structure comprising three semiconductor layers (26, 28) selectively formed on a main surface of the first conductivity type semiconductor substrate,

the three semiconductor layers including a second conductivity type (P-type) semiconductor layer (28) and two first conductivity type semiconductor layers (26) formed to interpose the second conductivity type semiconductor layer from both side surfaces (fig. 12),

a p-n junction boundary between the second conductivity type semiconductor layer and the first conductivity type semiconductor layer (28 and 26) (as best interpreted

by the Office) being substantially vertical to the main surface of the first conductivity type semiconductor substrate,

a second conductivity type base layer (30) formed on an upper surface of the second conductivity type semiconductor layer (28) and having an impurity concentration higher than the second conductivity type semiconductor layer (pg. 4, [0075]) (it is inherent that the base layer (30) has higher concentration than p-type drift layer (28)).

a first conductivity type source diffusion layer (32) selectively formed on a surface of the second conductivity type base layer (30);

a gate insulating film (34) formed on the second conductivity type base layer (30) interposed between the first conductivity type source diffusion layer (32) and the first conductivity type semiconductor layer (26) (as best interpreted by the Office), and

a gate electrode (36) formed on the gate insulating film (pg. 6, [0094]-[0098]).

With respect to claim 2, Yamaguchi teaches the semiconductor device according to claim 1, as set forth above, wherein a concentration of a first conductivity type impurity in the first conductivity type semiconductor layer (26) (as best interpreted by the Office) is 3 to $18*10^{15}$(atoms/cm^3) and a concentration of a second conductivity type impurity in the second conductivity type semiconductor layer (28) is 0.2 to $8*10^{15}$(atoms/cm^3) (pg. 4, [0074]).

With respect to claim 4, Yamaguchi teaches the semiconductor device according to claim 1, as set forth above, wherein an inequality: (100 * |A-B|/A is greater than or equal to 5) is satisfied where A represents a total amount of a second conductivity type impurity in the second conductivity type semiconductor layer and B represents a total

amount of a first conductivity type impurity in the two first conductivity type semiconductor layers (pg. 4, [0074]).

With respect to claim 9, Yamaguchi teaches the semiconductor device according to claim 1, as set forth above, wherein a plurality of unit cells identical to the unit cell are formed such as to employ the first conductivity type semiconductor substrate (20) as a common first conductivity type drain layer (fig. 12) and a termination structure is provided in which one of the first conductivity type and second conductivity type semiconductor layers (26 and 27) on a terminal portion of the first conductivity type semiconductor substrate (20) is connected to a unit cell that is closest to the terminal portion via an insulating film (66) formed on the first conductivity type semiconductor substrate (pg. 6, [0096]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi et al. ('083), as applied to claims 1 and 15 above, respectively, and further in view of Krumrey et al. (US 2003/0222297).

With respect to claim 12, Onishi teaches the semiconductor device according to claim 1, as set forth above, wherein a plurality of unit cells identical to the unit cell are

formed such as to employ the first conductivity type semiconductor substrate (11) as a common first conductivity type drain layer (fig. 1b),

Thus, Onishi teaches all the limitations of the claim, with the exception of explicitly disclosing:

a first gate wiring for the gate electrodes of the unit cells are provided in a peripheral portion of an element region that contains the unit cells, and a second gate wiring for the gate electrodes of the unit cells, which extend from the peripheral portion of the element region towards an inside of the element region, are connected to the first gate wiring.

However, Krumrey teaches gate wiring for a semiconductor device (figs.1A and 1B), wherein a first gate wiring (20) for the gate electrodes of the unit cells (3) are provided in a peripheral portion of an element region (2) that contains the unit cells, and

a second gate wiring (201) for the gate electrodes of the unit cells, which extend from the peripheral portion of the element region towards an inside of the element region, are connected to the first gate wiring (pg. 4, [0051]-[0060]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Onishi to include a first and second gate wiring structure, as taught by Krumrey, for the purpose improving the device and manufacturing process by saving space (such as the chip area) and enhancing topologic convenience (pg. 1, [0015]; pg. 4, [0064]).

With respect to claim 13, Onishi and Krumrey teaches the semiconductor device according to claims 1 and 12, as set forth above, and Krumrey further teaches wherein

the unit cells (3) are absent in the element region located underneath the second gate wiring (201) (fig. 1A).

With respect to claim 14, Onishi and Krumrey teaches the semiconductor device according to claims 1, 12, and 13, as set forth above, and Krumrey further teaches (fig. 1A) wherein the semiconductor structure (as best interpreted by the Office) that is physically separated from the unit cell (3) by the separating member (91), is formed in the element region located underneath the second gate wiring (201).

With respect to claim 16, Onishi teaches the semiconductor device according to claims 1 and 15, as set forth above, and Krumrey teaches wherein a gate wiring structure (201) is formed on the termination region (fig. 1A).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

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PRIMARY EXAMINER